**Project Description – Project Proposals**

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**Algorithms and Methods for On-Chip Information Fusion in Processor-based Designs – “AmonPro”**

**Project Description**

Information fusion (IFU) is a recent research topic in data analytics and diagnosis. Applications are found in automotive, machine engineering or process plant engineering [Mön17]. The fact is that IFU has the research potential for other fields such as microelectronics. The aim of this research project is the scientific investigation regarding the adaptation of IFU approaches into the systems arranged around processors. By our scientific study, we focus on the questions how algorithms, developed for the kind of large scales and dimensions such as factories or plants, can be adapted into microprocessors on the level of on-chip sensors.

Data analytics and diagnosis algorithms for monitoring or maintenance evaluate system states incorporating information from different sources. These may be several different visual and acoustic sensors like image, audio, or video sensors, and basic physical measures such as pressure, temperature or humidity. Moreover, the information can include specific process parameters such as throughput, utilized capacity, or production error rate. In addition, information from complex heterogeneous data types is incorporated. These may contain structured, unstructured, and semi-structured data, e.g., tabular data from relational databases, text data, hypertexts, and others. The heterogeneous data is aggregated by information fusion methods with the objective to recognize the characteristics of complex systems in real-time. For example, it enables the recognition of faults, anomalies or suboptimal executions, which arise from defects or environmental or in-system changes of some among the various different machine components. It allows monitoring, maintenance and sufficiently early reactions on the system conditions which is important for efficient handlings and consecutive operation of the system.

Through the adaptation of IFU approaches for single-core, multi-core (incorporating 2-10 processing cores) and many-core (hundreds or thousands of cores) processors around on-chip scales and dimensions, these systems are expected to benefit in the corresponding way as it is the case in systems represented by machineries or factories. The issues that need to be solved are with respect to the questions: how established methods should be adapted or extended or new methods are required, and how information from different on-chip data sources should be used to determine different system states by aggregation and evaluation. The fact is that optimizations are possible. It is motivated by the research findings on efficiency improvements based on the determination of an application state [GSC+15], [SKK16].

In-system sensors provide physical values such as local temperature, current consumption, and process values, for instance instructions per cycle (CPI), as well as cache hits and misses. Besides such standard variables, here research approaches for the analyzing additional variables are necessary. In [KhD15], the authors show the benefit of analyzing processed data, in comparison to traditional performance measurement approaches. Other approaches research the analysis of different values with promising results [KhD13], [ChL06], [SKK13]. Investigated approaches focus on a single value or set of values, but not in the way of IFU fundamentals. To the best of our knowledge, there is no approach which fuses multiple values. By the fusion of these in-system measured values, we aim to enable a more fine-grained and reliablestate determination. Within the scope of this research project, we focus on the analysis of the fusion of mentioned above conventional values, as well as less ordinary values, such as instance frequency of instructions or data and resources conflict frequency.

By the incorporation of IFU approaches, we concentrate on the determination of the processor state with the goal to achieve the possibility to induce a reaction. The results of the deeper and wider analysis in this direction are applicable to reconfigure the processor, its pipeline, cache, other components, or peripherals, in order to be optimized for the current state. With respect to the overall application, the processor’s behavior is tunable to achieve reduced power consumption. Goswami, et al show, that a comprehensive monitoring is possible with minor overheads [GCJ17]. The optimization of the processor itself is not in the scope of the project, however, the research delivers valuable results to the community working on the topic of runtime-adaptive processors.

In this project, we analyze information retrieval mechanisms (including signal pre-processing and feature extraction algorithms), attribute definitions, parameter settings and their efficient numerical implementations. Theories, originated from scales and dimensions of the systems represented, e.g., by manufacture facility, will be investigated in an environment, which is described by on-chip scales and dimensions. Due to the fact that, regarding on-chip characteristics, there is no comparable scientific investigations, the complexity of such task is challenging to pre-estimate. These estimations are to determine during the research activities of this project. Furthermore, approaches for on-chip data acquisition and the evaluation of the system state based on the fused acquired data will be analyzed. Both analyses will be executed with respect to the processor runtime optimization. Besides the approaches for data acquisition, the integration of the IFU algorithms will be investigated. Therefore, it will be necessary to analyze the performance requirements of the IFU algorithms, as well as the performance impact of sensors for the data acquisition. The challenge will be to enable our targeted advanced monitoring with as little overhead in resources usage as possible.

Throughout our approach, the IFU algorithms will be studied in an environment, where the data is fully different and in another correlation as in the commonly investigated scales and dimensions. Moreover, the data acquisition of processors will be evaluated to meet the demands of the IFU algorithms. Finally, the requirements, in terms of processing of measured values and measurement performance, and the potential for an advanced state determination will be investigated. In the domain of system architectures and management, the knowledge acquired within this research project will be a valuable input in order to develop optimized processors with a fixed architecture and to apply our techniques and methods for run-time adaptive processor architectures.

# State of the art and preliminary work

This project has its roots in yet unrelated fields of research. One field is the management of processors during runtime which is a current research topic of Prof. Dr.-Ing. habil. Michael Hübner [MoH16], [NMH+17], [JFK+17]. The other fields are algorithms for data analysis and information fusion which are current research topics of Prof. Dr.-Ing. Volker Lohweg [EML16], [FMH+17], [HML17], [HML17b]. The combination of these two fields is a promising approach to advance the efficiency of processors by introducing data analysis and fusion algorithms in the management systems of processors.

The guarantee of the success of this project is predicated on the previous and current collaborations of both institutions. It involves joint excellent research [MDL+16], finished [Mön17] and actually running PhD programs as well as partnerships in research projects (e.g., Federal Ministry of Education and Research Grant FNR 03FH040PX5 (smartBN) and Grant 16ES0391(DnSPro)).

A necessary factor for the success of research is deep understanding of basics and current state of art in both fields. Therefore, the following Section 1.a will present the state of art in the field of processors, which is investigated by the researchers of Ruhr-University Bochum. The state of art in the field of data analysis and fusion algorithms, investigated by the researchers of inIT, is presented in Section 1.b.

## Management and Monitoring of Processors

The effort of managing processors in order to operate them efficiently is increasing in all its subtasks, starting with the monitoring of the system state, followed by its evaluation, and the action taken based on the evaluation. The increase is caused by different aspects of the systems themselves and their application.

One aspect is the mobility and ubiquity of today’s computing systems. The processor inside such systems has to meet strict power constraints, as well as satisfy the applications performance requirements. Optimizing the system offline can be insufficient, as the performance requirement depend on the application’s execution phase [SKK13]. Another aspect is the increasing performance of processors, enabling the consolidation of several applications onto a single unit. This causes scenarios in which applications with different criticalities are sharing the same processor. Moreover, applications may be loaded and unloaded during runtime, e.g., by requests of other entities such as a user. Thus, dynamic mixed-critical systems are the consequence [Hei11].

Besides these application-related aspects, there are other reasons for an aggravated management, as for instance the heterogeneity of today’s computing systems. Processors can contain dedicated accelerators in order to increase their efficiency and performance. There are several examples for this trend in the academic world as well as in industry. Research projects such as FlexTiles[[1]](#footnote-2) or EURETILE[[2]](#footnote-3) investigate, among other aspects, into new heterogeneous architectures. But also commercial products, as for instance ARM’s bigLITTLE technology [CKH15] or Xilinx’s Zynq chips [ARG+13] are heterogeneous to enable an increased efficiency and performance. Zynq is also reconfigurable during runtime, as it contains programmable logic, which can also be found in field programmable gate arrays (FPGAs). Even though common processing systems are currently only reconfigurable during runtime through software updates, the next generation of processing systems, which is currently investigated in the academia, will be reconfigurable on the hardware level as well. Research projects in this area are for instance the R3TOS project [Ite13] or the ReconOS project [Age14].

The heterogeneity and re-configurability in software and hardware enable a system to take action and adapt its processing according to its state in the field. As shown in this section, the research community has come up with several promising approaches on how to take action.

Within the scope of this project we will investigate into the monitoring of the system state and system state evaluation. Therefore, the following subsection 1.a.a describes current research efforts within the field of system monitoring. The following two subsections 1.a.b and 1.a.c discuss the state of art in the field of reconfigurable processors and scheduling in reconfigurable systems. Both topics are of high relevance for the evaluation of the system’s state, which is the link between monitoring and action taking.

## Monitoring Processors

Monitoring of processors and processor systems is a well understood and investigated topic. Halsall and Hui described the rationale and the design of a performance monitoring system for embedded computing systems [HaH87]. System-related and application-specific events can be recorded through software functions. Today, advanced hardware-support for monitoring is available; enabling more sophisticated monitoring with less overhead and new parameters as for instance power consumption. This hardware support is well-known and applied, for instance in the FlexTiles project. Within this project, the application-execution can be adapted to increase the system efficiency [LMA+12]. Besides the FlexTiles project, there are several other projects looking into the information extraction and evaluation in processors, as well as how to process this information. The System-/Physician-on-a-Chip (SPOC) project, for instance, is funded by the DFG and investigates into the monitoring of integrated circuits on transistor and physical level and their online adaptation [DFG15]. In contrast to the proposed project, the physical effects like for example defects on transistor level are in focus, while this project uses higher-level information of a processor-based system to derive information. However, it is of great interest to cooperate with the researcher of the System-Physician-on-a-Chip (SPOC) project and connect also to their results of the investigation.

In addition to research projects, monitoring is also available in commercial products. The current Intel processors Intel i7 or Xeon E7 for instance contain, among others, a monitoring facility denoted as performance monitor unit (PMU) that supports monitoring of several processor and general system parameters. Saini et al. use the PMU for performance analysis of a computational fluid dynamics application [SMT+11]. In general, the monitoring capabilities provided for Intel and AMD processors is a very valuable source of information and will be used for investigations within this project regarding the exploitability of our information fusion approach on such complex processors. With other commercial processor cores, like Tensilica, performance counter and the trace buffer modules can be used to perform the investigation on for modern embedded systems. The Tensilica IP is available for both research groups.

## Reconfigurable Processors and Processing Systems

Adaptive computer systems exploit the heterogeneity to dynamically execute tasks more efficiently than in a homogeneous system [Pae15] with respect to the runtime state. Moreover, the re-configurability allows adapting the system dynamically on the hardware level. Adaptations on this level may include dynamic voltage and frequency scaling (DVFS) or a modification of the instruction set (IS) to better fit the executed application. The state of the art is presented in the following text.

Optimizing the IS of a processor for a specific application would imply adding more complex instructions that result in a physically bigger and more complex chip. Moreover, the operation frequency would be reduced. Thus, other tasks, which do not benefit from the complex instructions, may be decelerated. A runtime-adaptable IS would support several applications. But this will lead to new challenges at two design levels: register-transfer level (RTL) implementation and software compilation. As partial reconfiguration technology for FPGAs has been offered for the last decade, runtime modifications at the RTL level became realizable for any part of a soft-core processor, i.e., a processor which runs on a FPGA. However, the challenge to handle the reconfiguration and adaptability at the compiler level has been another main obstacle. Therefore, most of the research in this area mitigated the problem by trying to extend the IS at runtime instead of modifying it.

The authors of [Hue12] propose a reconfigurable soft-core processor architecture, which utilizes the internal configuration access port of Xilinx FPGAs to configure the logic during runtime and to additionally write and read processing data to and from the FPGA internal memory. Thus, the architecture of the presented general purpose processor can be optimized for the execution of a specific application.

The authors of [BSH08] and [PLF06] propose approaches similar to the previous one: the invasive Core (i-Core), respectively the extensible microprocessor without interlocked pipeline stages (eMIPS). The i-Core implements a core IS and an extension for the IS. The functionality of the IS extension is implemented in a reconfigurable fabric and prepared during compile time. The IS extension can also be executed as a sequence of the IS core. Therefore, the decision whether to use the IS extension or not can be made during runtime. By optimizing the application execution with this method a speedup factor of 22 has been achieved for a single task video encoder for the H.264 codec. A similar approach has been followed within the eMIPS project. The application’s instructions are tracked during execution and the system tries to identify the most often used basic blocks in order to create a new IS extension which is optimized for its execution. The eMIPS approach also utilizes reconfigurable fabric in order to adapt dynamically at runtime.

The data processing architecture eXtreme Processing Platform (XPP-III) [BeV04] is a heterogeneous architecture, which offers logic for dataflow and logic for control-flow oriented processing. Depending on the application needs and workload of the processing elements, the execution of the application can be optimized during runtime. The CHAMELEON heterogeneous system on chip (SoC) consists of a general purpose processor, a fine-grained reconfigurable area, and the MONTIUM sub-architecture [HeS03]. MONTIUM is a coarse-grained reconfigurable architecture and was designed to offer a balance solution between flexibility and energy-efficiency for digital signal processing applications. Another heterogeneous reconfigurable architecture was developed within the FlexTiles project [Jae15]. It contains a heterogeneous many-core bottom layer and an FPGA layer stacked on top of it. Within the context of this project a toolflow to develop applications for this architecture, as well as a runtime software has been developed. The runtime software supports to dynamically load and unload applications, as well as change the resource assignment.

As the processor workload varies with the execution phases of an application [SKK13] another idea is to apply DVFS. Nunez-Yanez and Beldachi show in [NuB14] that the implementation overhead for a Xilinx Zynq hybrid-chip, which contains static and reconfigurable logic, is in the range of only 1.6 % for flip-flops and 3.3 % for the look-up tables. In [PiS01] three different approaches to schedule DVFS in real-time (RT) applications are introduced: static voltage scaling, cycle-conserving RT-DVFS, and look-ahead RT-DVFS. The authors present simulation results, which show that depending on the scheme the system’s energy efficiency can be improved by around 20 % to 40 %.

## Scheduling for Reconfigurable Processors and Processor Systems

In reconfigurable systems the scheduling problem is of temporal and spatial nature, as the scheduler needs to decide when and where to schedule a task. Current research shows different possibilities to schedule a task set to a reconfigurable system. Saha et al. propose the periodic RT scheduling strategies called DPSFR (Deadline Partitioning Scheduler for Fully Reconfigurable Systems) and DPSPR (Deadline Partitioning Scheduler for Partially Reconfigurable Systems) [SSC15]. Both scheduling strategies aim to achieve high resource utilization while also minimizing the task rejection rates, which occur when a RT constraint is not met. DPSFR targets systems, which are reconfigured as a whole, whereas DPSPR takes individual reconfigurable fabric into account. Thus, these approaches target reconfigurable systems only. A hybrid system containing a general purpose processor and reconfigurable logic slots for dedicated processing modules is targeted by the approach of Pan and Wells [PaW08]. They propose a dynamic task scheduling algorithm for reconfigurable SoCs and show that their dynamic scheduling approach outperforms a static approach when it comes to a certain degree of system complexity.

## Conclusion

Current processors are already flexible in order to allow dynamic adaptation to a runtime state. Future approaches will advance this flexibility by far, as it is shown by current research projects.

However, to exploit this ability, sophisticated monitoring, fusion, and evaluation of the state is necessary. An improvement of these aspects would strengthen the basis for dynamic online adaptations and enable better utilization of the provided flexibility. Until now, an approach investigating into new ways to monitor the state through novel ways of data sampling is missing. This includes the utilization of new high-level data sources (pipeline stalls, cache hits/misses, etc.) with respect to complex relationships on chip level, which differentiates this project from [DFG15]. Moreover, such an approach calls for, but also enables, new methods for the processing and evaluation of recorded data, which need to be researched.

## Data Analysis and Information Fusion (Algorithms)

The main intention of *data analysis* is discovering of useful information. Information fusion is a technique, which is able to extract knowledge from the information. In many domains of applications such knowledge is required for the description of a system and its handling, e.g., for modeling, condition monitoring, phenomena prediction of the system, etc. Within the project we concentrate on the discovering of information from a feature extraction and feature selection point of view (for modeling of the system) with sound priority to the accurate and robust classifier design (for condition monitoring or phenomena prediction). In addition, fast computational execution time for the description and handling of the system is and will have significant priority within our research [ToL15], [DöL14], [DöL15], [DML14], [ToL17], [ToL18]. Furthermore, the combination of data analysis and IFU principles with respect to the mentioned priorities will be investigated.

Considering information discovery, classifier design and computational capability, there is nowadays a clear tendency in data analysis research. It is characterized by efficient feature extraction and feature selection models [RiW14], or/and by simplicity and robustness of the decision making model [JiC15], and fast execution time [GuB15]. Many fields of mentioned scientific development progressions are originated from the demands of modern industry-driven applications and environments (especially in the terms of complex systems like Cyber-Physical-Production Systems [NiL15]), and from demands of complex database system processing (e. g., “Big Data” management [GGO+13]).

IFU is a widely investigated concept with a large number of scientific frameworks. With respect to technical systems, IFU has gained more attention starting in the 1970s when new sensors, advanced processing techniques, and increasingly powerful processing hardware became available. Starting then, appropriate data processing models and fusion algorithms have been driven nearly exclusively by applications in the military defense sector. During the 1990s and early 2000s, those algorithms have been adopted by the civil sector for usage in industrial fault diagnosis and condition monitoring applications [HaL01]. A standard fusion definition has been introduced by Steinberg and Bowman [StB01]: “Information fusion is the process of combining data or information to estimate or predict entity states.” It is, in other words, the process to transform data coming from different sources into knowledge, where ordered data in a certain context generates information, which results in knowledge when it is properly aggregated with respect to the situation or problem of interest [AyK06]**.** Deep system understanding is inevitable throughout the whole process [HaL01]. Recent research regarding information fusion is carried out in the industrial context, in traffic modeling scenarios, military, as well as in the home care sector (ambient assisted living (AAL)).

Khaleghi et al. identify in their review article [KKK+11] a number of main challenges posed on IFU approaches arising from its input data. These are data dimensionality, data imperfection (like uncertainty), outliers and spurious data, conflicting data, data modality, data correlation or missing data, and more. Thereupon, we have to face difficulties with the respect to processing framework, operational timing, and static vs. dynamic phenomena. The aforementioned challenges meet in a natural manner many data analysis hurdles, which will be addressed together with IFU principles by our research strategy. Regarding these topics, we describe the scientific state of the art for our research prospects in more details below.

## Data Analysis

In many cases, data analysis workflows include following steps: (1) feature extraction, (2) standardization to make features with different scales comparable, (3) normalization to achieve the same range for all features, (4) signal or image-processing filtering to improve the signal-to-noise ratio [Lyo11], [Wal08], (5) feature selection, which might lead to dimensionality reduction.

The determination of the system’s condition is a process of monitoring the operating characteristics (in our nomenclature *features*) of the system. Changes of the monitored data are suitable to estimate the current condition of the system and predict the need for maintenance before serious deterioration occurs. The generated data volume in such systems might be large, complex, or not completely understood. Therefore, the extraction of meaningful features might be not an easy task. The beginning of investigations starts by converting raw data into a set of useful features within, e. g., existing classical feature extraction and selection methods (cf. histogram analysis of feature distributions of raw or filtered data or their combinations, RELIEF algorithm for feature selection [KiR92], Linear Discriminant Analysis (LDA), Principal Component Analysis (PCA) or Multidimensional Scaling (MDS) [KrW09]). Extracted and selected features have to be analyzed with respect to the required performance of the system. For example, suitable is feature ranking, which uses a measure instead of the error rate to score a feature set which is chosen to be fast to compute, whilst still capturing the usefulness of the feature set. Common measures include the mutual information [PLD05], Pearson correlation coefficient [BCH+09], or the scores of significance tests [Koh05] for each feature combination.

Mentioned above Linear Discriminant Analysis (LDA) and Principal Component Analysis (PCA) originated methods belong to so-named filter methods. They operate, e. g., with statistical characteristics, ranking, and scoring of features or their combinations. Such methods are often fast; however, in many cases the resulting performance might be weak. In addition to filters, wrapper and embedded methods can be considered [KoJ97]. They utilize classifiers to score feature subsets according to their predictive power. Such methods might be computationally very intensive, but usually provide the high performing feature set. Embedded methods [ZHG+13] perform feature selection in the training process and are specific to given learning machines. These techniques tend to be between filters and wrappers in terms of computational complexity. Their incorporations, called hybrid methods, use a filter to rank the features, and then feature subsets are computed following a wrapper.

Feature selection is a very important part of the data analysis workflow. Many of the feature selection procedures lead to dimensionality reduction. Dimensionality reduction is an essential topic for our research activities and will be discussed in more details below.

One of the major problems in analyzing complex data stems from the number of variables involved. Analysis with a large number of variables generally requires a large amount of memory and computation power. Moreover, it might result in a classification algorithm which generalizes poorly to unknown samples. Feature selection principles might be able to reduce number of features or construct their combinations to get around these problems while still describing the data with sufficient accuracy. The quality of condition monitoring techniques and their applicability are determined by the effectiveness and efficiency, with which characteristic features are extracted and identified. In terms of dimensionality reduction, feature selection pursues the following goals: (1) reduction of computation time and space required executing the algorithms and (2) improvement of classifiers by feature combinations or removal of irrelevant features. For this reason, a deep system understanding is necessary to choose the appropriate features.

Established strategies and algorithms for processing large amounts of data are not studied on the on-chip systems now. Applying algorithms for industrial production processes to the measurement values of a processor incorporates known research areas into a new research field. Both, industrial systems as well as on-chip systems will benefit from symbiosis effects.

## Information Fusion

In many cases the information captured from sensors is imprecise, incomplete, or inconsistent. Moreover, sources are not reliable [BSW06]. Therefore, it is necessary to apply fusion concepts, which are able to handle and measure imprecision and (un-)reliability, named here as *uncertainty*. There are two major types of uncertainty [AyK06]**.** One class is *aleatory*. This type is characterized by its random and non-deterministic nature and thus represents the inherent randomness of a problem. The second class is *epistemic* uncertainty, also denoted as subjective uncertainty. Its source is the lack of knowledge due to incomplete data. Often, such uncertainty cannot be avoided, especially when it comes to real-world applications [KlW99].

The basic demand to process uncertainty accordingly is the application of methods and tools to model the available information. These methods serve for data transformation into a common processing frame [KKK+11]. In [AyK06] authors propose the framework of *probability theory* in case uncertainty is quantifiable. They admit that epistemic uncertainty can only be modeled with additional effort as a probabilistic variable. Uncertainty is often recognized, but cannot be expressed in statistical or probabilistic terms. In order to handle epistemic uncertainties connected with such problems, information models based on *Dempster-Shafer theory of evidence* and *fuzzy set theory* are adequate approaches.

The techniques modeling aleatory uncertainty are based on *probability theory* (ProbT). *Frequentist probability* is based on repetitions of an experiment, observation, etc. under identical conditions. It relies on sampling only and provides no means to include prior or expert knowledge. These drawbacks are eliminated in the framework of *Bayesian probability* [Jay03]. *Bayesian fusion* is the most prominent probabilistic fusion method and is well studied both theoretically and practically (cf. [Jay03], [Bis09], [KKK+11]). All methods based on Bayesian fusion assume that data are acquired from independent sources, whose statistical behavior is identical [Kál60], [Del96], [SGL15]. Additionally, the prior must be determined before any application. This is a nontrivial task, especially in application fields where no statistical information is available [Zad62].

*Condition monitoring* is a hot application area in current fusion research. A fusion method based on probabilistic finite state automata is presented in [SSV+14] and [PCJ+14]. The model is learned from captured time series for semantic model generation of a distributed application. It works on hidden Markov models, which were extended such that the applied probabilities are replaced by *Dempster-Shafer theory's* basic belief assignments.

The *Dempster-Shafer theory of evidence* (DST) is a theory, which is applied to express degrees of belief about propositions quantitatively. *Dempster’s rule of combination* (DRC) from [Dem67] was put into new context. It combines *degrees of belief* to the same proposition originating from different sources [Sha76], [AyK06]. The degrees of belief are based on assigning *upper* and *lower probability* bounds to a proposition from the frame of discernment to quantify a state of partial knowledge. In DST, these measures are denoted *belief* and *plausibility*. It is not necessary to assign a degree of belief to every element in DST. Included was a *measure of conflict* between beliefs in DRC. Due to possible counterintuitive results in conflicting situations [Zad84], a number of alternative combination rules appeared [KKK+11]. In addition, exponential time complexity problem with respect to the number of beliefs to combine [Bar81] has to be solved efficiently. A recent theoretical framework serving as a generalization of DST referred to as *Dezert-Smarandache theory of paradoxical reasoning* (DSmT) was introduced in [Dez02].

The importance of DST is manifested in a large number of successful information fusion applications known in literature. To the most recent belong applications in condition monitoring of technical systems (cf. [Cho13], [QLP14], [WTL14], [Krü15]). Authors emphasize, that the theoretical foundations have been advantageous in ambiguous and conflicting situations over other approaches, e. g., based on ProbT.

*Fuzzy set theory* (FST) has been constituted by Zadeh [Zad65]. He considers sets with unsharp boundaries and denotes these as *fuzzy sets*, “a ‘class’ with a continuum of grades of membership” [Zad65]. These sets are used to model uncertainties, which arise from imprecisions. Each fuzzy set is characterized by a *membership function*. *Fuzzy aggregation operators* serve for the aggregation (or fusion) of several membership functions. All of these operators have not been invented specifically for FST. Instead, they are accepted mathematical operators, which are also applicable to fuzzy sets [Yag88].

Fuzzy models have successfully been applied in IFU problems of various application fields. A malware detection concept for Android mobile phones based on fuzzy pattern analysis was presented by [ASH+14]. Another diagnosis task is described in [AIK14], which deals with the monitoring of electrical transformers. Advantageous application of a fuzzified DST approach to support diagnosis in a medical context was presented [Str15].

## Sensor and Information conflicts

In processes a vast variety of different sensors is increasingly used to measure and control technical systems, machines, and different physical, chemical and biological processes. One way to handle the resulting large amount of data created by hundreds or even thousands of different sensors or information sources in an application is to employ information fusion systems [MöL14]. Information fusion systems, e. g., for condition monitoring combine different sources of information, like sensors, to generate the state of a complex system. The result of such an information fusion process is regarded as a health indicator of a complex system [MöT+15].Therefore, information fusion approaches are applied to, e.g., automatically inform about a reduction in defined quality, or detect possibly anomalous situations. Considering the importance of sensors in the previously described information fusion systems and in processes in general, a defective sensor has several negative consequences. It may lead to failures, e.g., when wear and tear effects is not detected sufficiently in advance [MöV+12]. Therefore, it is necessary to detect faulty sensors to reduce information conflicts by computing the consistency between sensor and data values. Consistency analysis is one of the most underdetermined issues in technical systems [Mön17], [HML17].

## Conclusion

The analysis of the state of the art shows, that flexible processor architectures as well as approaches for monitoring of different physical and processor state related data on chip are available, but are not consequently exploited for data fusion in order to derive an increase of information about the system status. Especially methods and algorithms for information fusion are not well investigated and exploited in the scenario, where data from processor architectures are delivered from on-chip sensors. The researchers expect as a result of the investigations within this project the deep understanding of the relation between processor status data, which have not been recognized before.

## Project Related Publications and Patents

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# Objectives and work programme

## Anticipated total duration of the project

The anticipated duration of the project is three years. It is envisioned that two PhD candidates (one at inIT, one at ESIT) work on complementary research topics and finalize their PhD within this time frame. At inIT, the research focus lies on the algorithms for information fusion while the topic of the research at ESIT focuses on the processor level with data acquisition including the on-chip sensors. During the project phase, the PhD candidates work as team and exchange on a regular basis their current state of research and results. It is also envisioned, that the PhD candidates work intensively together during visits at inIT and ESIT where they discuss the research of their specific topic and present their work to other PhD candidates in order to receive feedback. Frequent project meetings with Prof. Lohweg and Prof. Hübner guide both PhD candidates and help to keep the scientific goals of this project in focus.

## Objectives

The objective of this project is to research new methods for the run-time monitoring of processors, based on incorporation of IFU theoretical fundamentals. Our goal is to enhance the monitoring, to determine the processor’s state more fine-grained, reliable and in advance. Thereby, we will improve and advance the possibilities of predictive actions, such as branch prediction or speculative execution, to enable performance gains. In addition, these enhancements will indirectly increase the efficiency of processors, by laying the foundation for a more optimized adaptation of the processor’s hardware and software during design, as well as runtime, and to support decisions also e.g. in exception handling. With a reliable prediction, speculative actions within the core can be done more efficient and new possibilities, such as predictive maintenance in the area of processors, become possible. To achieve our goal, of an enhanced state determination, we identified multiple research tasks.

First, we will evaluate the possibilities to acquire measurement data inside the processor, analyze the feature extraction and feature selection fundamentals and emphasize promising values to be measured and processes by the IFU techniques. We will use existing complex architectures like Intel and AMD processors with their ability to monitor the cores in order to perform first investigations and to evaluate, which other information would be beneficial for a state prediction. These are most probably values generated deep in the processor architectures like e.g. individual states in the pipeline stages or wait states for memory accesses.

Therefore, hardware architecture and software architecture will be chosen, and the possibilities for data acquisition will be analyzed. For the analysis with respect to our aims, a deep understanding of architectures is necessary, to enable an adequate data acquisition through sensors. The result of this analysis is the set of values from existing data sources and possible values from additional sensors. These results will be the basis for a *sensor concept*. The sensor concept describes the sensors, their properties and the implementation. This concept will be refined through the whole project research activities. Moreover, the process of feature extraction and feature selection is analyzed for the application of IFU fundamentals in the targeted processors. This analysis will lead to a preliminary set of IFU algorithms that will be analyzed further.

Since we cannot integrate additional sensors in industrial high-end processors, we need a state of the art processor architecture with an open hardware model in order to perform evaluations of our solutions. We selected the RISC-V[[3]](#footnote-4) instruction set architecture (ISA), since it is a upcoming industrial standard for embedded systems and it is public available. Ii is an open source that has been developed at the University of California, Berkeley, and has become one of the standard open ISAs for industry and academia. Thus, results obtained on this ISA will have a direct impact on a large community. In addition, the RISC-V provides a mature ISA. It is suitable for large and small platforms, as well as FPGA and ASIC implementations. A good example for this versatility is the Parallel Ultra Low Power Platform developed at the ETH Zurich and University of Bologna. An ongoing cooperation with the group around Prof. Benini at ETH Zurich enables access to ASIC-based RISC-V performance evaluations to tests of the approaches from this project.

ESIT observes the research field of ISAs as part of its general research activities. Within the first phase of the project it is planned to review the state of art based on the continuous observation at ESIT. Based on the results, the final target architecture for this project will be chosen.

The software architecture will be based on an operating system. This means, we investigate in the realization of the IFU algorithms first using software, and with an FPGA-based prototype, and a hardware/software co-design approach where we identify parts of the algorithm which can be realized using reconfigurable hardware. This approach will enable us to deliver more relevant results, as well as potential benefits for the IFU algorithm implementation in operating system services and processor peripherals. We have two candidates that can be used within this project. An embedded Linux based on Yocto[[4]](#footnote-5) or the real-time operating system FreeRTOS[[5]](#footnote-6). A Linux-oriented approach would support additionally the Intel and AMD cores which we use for the initial investigations. The final choice of the operating system will be based on the hardware architecture and the sensor concept. We focus on open source benchmarks suitable for embedded systems. Among other we plan to use the embedded benchmark suit MiBench developed at the University of Michigan [GRE+01].

Second, we will integrate sensors for data acquisition into the RISC-V processor and evaluate the state information based on fused data. Therefore, an optimized placement of data sources within the processor will be investigated into. The integration will be done within the processor model to be available in simulation, as well as possible prototyping on FPGAs. The optimization will be investigated with respect to a minimal influence on the processor’s performance and power consumption. The coherencies between the acquired values are analyzed. Detection of data sources leading to information conflicts is processed. Based on this analysis, suitable IFU algorithms will be evaluated and adapted to be integrated into the architecture.

Third, we will evaluate the integrated system and analyze the results. Therefore, multiple test scenarios will be developed, and the performance of our approach will be analyzed. The test scenarios will be based on the execution of different benchmarks like MiBench [GRE+01]. Within the evaluation, the state determination behavior under the influence of inference will be tested.

In summary, this work will extend the knowledge about analyzing the state of processors all the way from gathering the information, through their processing, and the interpretation of the results. Therefore, this research project will pool expert knowledge from the research field of processors as well as the research field of algorithms for data analysis and fusion. With this combination, new ways for an improved system monitoring will be researched, enabling more efficient processors. The project will deliver highly valuable scientific results into different research domains. First the domain of processor architecture, since the interrelations of information derived from unconventional data sources within a processor is exploited. Second the domain of IFU, since algorithms and methods from the established systems are exploited into the new environment of on-chip data. And third, to the community of adaptive processor systems since all research results can be used to adapt more efficiently in future reconfigurable systems and by using with novel cost functions to decide when a system update needs to be done.

## Work programme incl. proposed research methods

The research assistant person 1 (P1) and person 2 (P2) should have the opportunity to graduate. For that reason, the entire topic is subdivided into four partitions.

P1 works on the topic „information fusion“.

P2 works on the topic „methods of hardware monitoring and system state determination“.

The following tables demonstrate the planned tasks in the work packages (WP), objectives, results and staff effort in person months.

**WP 1: Requirement analysis for method of on chip-data acquisition and information fusion**

|  |  |  |  |
| --- | --- | --- | --- |
| **Staff effort (person months)** | 13 | **Employee** | P1 (100%) and P2 (100%) |
| **Objectives** | | | |
| Evaluation of data acquisition of existing complex processors like Intel and AMD using approaches like e.g. the Intel Machine Check Architecture. Additionally, the targeted hardware and software platform of RISV-V and its capability to be extended through sensors will be performed. This activity leads to a general sensor concept. The sensor concept contains the possible sensors and their properties. Its development will be continued in following WPs. Evaluation of feature extraction and feature selection methods, as well as examination of suitable IFU algorithms.  The workpackage focuses mainly on 3 objectives:   * Exploration, analysis and realization methods of on-chip data sources which we call sensors or monitors. * Evaluation of feature extraction and feature selection techniques * Evaluation and selection of IFU algorithms | | | |
| **Description** | | | |
| **WP 1.1: Exploration of data acquisition**  In this WP, a short review of the current state of art in ISA research, based on the continuous research field done by ESIT, is conducted. The results of the review will determine the later hardware and software platform with RISC-V. Moreover, the data acquisition in the platform is explored. Therefore, we research the capabilities of hardware and software sensors, as well as their utilization for our approach. This analysis will target embedded-Linux-based platforms, as well as FreeRTOS-based platforms which are more relevant for low power embedded systems. The results of the analysis will be the basis for the sensor concept and will be used to evaluate the features for the IFU algorithms.  The sensor concept will include the possible on-chip sensors and their properties. The main properties will include the measurement performance, resource usage, and relation to other sensors. The sensor concept will also include state of the art opportunities for monitoring complex processor cores like Intel and AMD e.g.by using Intel’s machine check architecture. This enables a preliminary evaluation and an exploitation of our approaches with this processor architectures.  **WP 1.2: Evaluation of existing data analysis and information fusion algorithms concerning the implications for processor state data fusion**  Feature extraction and selection operations are necessary to reduce the number of variables to a range manageable in small-scale systems like processors. The contribution to the project will cover theoretical studies of the fundamentals to the extraction of powerful features, as well as investigations of feature selection principles regarding dimensionality reduction and performance of later decision making. Such topics as well as design of robust and accurate classifiers and fast computational execution time will be investigated. Furthermore, generalization ability, adaptation, and automation properties of the developed methods will be analyzed.  The information encoded in the features extracted and, if necessary, selected by the chosen algorithms is the base for the subsequently applied information fusion algorithms. These are analyzed concerning the implications for processor status data fusion. These works rely on the data sources identified in WP 1.1 and the features extracted from the data acquired from these. The characteristics of the data will be mapped onto the information fusion algorithms, which are considered to be applicable for on-chip condition monitoring. A multitude of possible fusion algorithms are possible and applicable. These originate from the information models described in Section 1.b.b. The multilayer attribute-based conflict-reducing observation system (MACRO) for information fusion concerning condition monitoring of complex systems will be adopted to chip behavior [Mön17]. It is considered as a useful basis to the application of information fusion in processors for condition monitoring. Its applicability is determined by tests on the data acquired from the data sources identified in WP 1.1. The findings of this WP serve as the basis for WP 2.2 to research the actual information fusion algorithm applicable for on-chip condition monitoring. | | | |
| **Results** | | | |
| Within WP 1, the hardware and software platform for this project will be determined. Moreover, a sensor concept for the monitoring of the values inside the processor will be developed for the target platform, based on existing techniques and their extensions. It contains hardware and software sensors, their data type, measurement rate and accuracy. In addition, the sensor concept gives an overview about current knowledge on how different values relate to each other, as well as an outlook to further opportunities with future architectures. A first evaluation of the sensor concept will be done by comparing it to the capabilities of system monitors coming from complex processor cores like Intel and AMD.  The sensor concept will be used in the studies of feature extraction and selection, conducted within WP 1. Moreover, the requirements of promising IFU algorithms and the capabilities of the platform will be matched, to develop a set of suitable algorithms. | | | |

**WP 2: Deployment of the algorithms and data acquisition methods**

|  |  |  |  |
| --- | --- | --- | --- |
| **Staff effort (person months)** | 21 | **Employee** | P1 (100%) and P2 (100%) |
| **Objectives** | | | |
| This workpackage is targeting two objectives:   * Performance and resource aware placement and integration of sensors into the processor architecture * Evaluation of state determination using IFU algorithms and analysis of the data source impact in relation to the data type, sampling rate, and correlation | | | |
| **Description** | | | |
| **WP 2.1: Integration of sensor concept and IFU algorithms**  In this WP, the sensor concept will be integrated into the RISC-V based platform. Within the integration we will research an optimized placement of the sensors into the processor hardware architecture. The optimization will be done with respect to the resource usage, and the requirements of the IFU algorithms. Platforms with different sensor configurations will be implemented to enable an evaluation of different sensor constellation and the IFU algorithms in WP2.2. The integration of sensors into the hardware platform will be done within the RISC-V processor model. This approach enables the prototyping with FPGAs.  In addition to the integration, the analysis of the relation and coherence of values acquired by different sensors will be continued. Based on the results, strategies for the test scenarios will be developed. Moreover, the analysis supports the IFU algorithms integration. The necessary interface for communicating the measured values to the IFU algorithm will be developed.  In preparation for the evaluation of the integrated platform, we develop comprehensive test scenarios. The evaluation itself requires the planning of test series, based on the scenarios, and the validation of the design of experiments (DoE) as well as the realization of the DoE. The tests will be performed in simulation environments  **WP 2.2: Evaluation of state determination based on IFU**  In this WP we investigate into the evaluation of the information about the processor’s state gained from the fused data source values, also under conflict. Their significance for the overall hardware state of the processor, as well as their significance for the state of executed software applications will be evaluated. Moreover, we will validate the results of the previously conducted experiments in the real-world environment on the physical test. Our goal is to use the state determination for existing and novel predictive activity on software and hardware level. One example is branch prediction which could benefit from a more filigree determination of the processor’s state. Another example is a more precise speculative execution using the information fusion approach. Novel methods are an enhanced instruction dispatching from the respective units in a superscalar processor. Additionally, the relation to Tomasulu’s scheme will be investigated.  The investigations in WP 1 result in a number of possible IFU algorithms that are suitable for on-chip condition monitoring. The algorithms will be validated and evaluated towards their actual applicability and performance in terms of robustness against variations of the data and state determination precision in this WP. All experiments are conducted on on-chip data within the environment prepared in WP 2.1. In order to evaluate the IFU algorithm, an investigation of the considered processor states and the expression of them against the backdrop – what can happen and how serious is the occurrence – are carried out. The relationships between the different states and the measured on-chip data will be analyzed. The analysis will take into account all available values, including the ones sampled with new data sources, which will be included in the processor’s architecture. Moreover, the acquired data is analyzed and interpreted regarding reliability. The algorithms have to contend with the acquired data of highly heterogeneous types: It will be from binary, discrete-valued, and value-continuous data as well as between event-driven, cyclic, acyclic, or time-continuous data. Each type of data has different characteristics and must be handled differently. The synchronization of the different data sources must also be considered and possible measures taken. The quality and plausibility of the fusion algorithm will be examined, weaknesses identified, and if necessary improved. It consequently leads to the definition of the most appropriate algorithm. | | | |
| **Result** | | | |
| Within WP 2, multiple configurations of our evaluation platform will be implemented. They contain the integrated sensors, as well as the IFU algorithms. The interface between sensors and IFU algorithms will be developed. Moreover, the test series for the evaluation will developed. The evaluation will be conducted within the WP and the analysis in WP 3 prepared. In addition, the research of the coherence of the sensor values will be continued and documented. | | | |

**WP 3: Scientific Analysis and Validation of the Results**

|  |  |  |  |
| --- | --- | --- | --- |
| **Staff effort (person months)** | 28 | **Employee** | P1 (100%) and P2 (100%) |
| **Objectives** | | | |
| This WP has mainly three objectives:   * The in-depth validation of the scientific approach according to its results from the previous workpackage * The formal description in terms of mathematical equations and/or pseudo-code of the derived results in order to deliver a basis for exploitation in more application-centric projects * Exhaustive tests and evaluation to combine the expertise gathered from the data source integration into the processor architecture and the used algorithms for information fusion * Exploitation for predictive mechanisms within processor cores in order to optimize performance and power consumption | | | |
| **Description** | | | |
| **WP 3.1: Analysis of the processor state prediction**  The focus of this WP lies on the analysis and the scientific discussion of the simulations results achieved in WP 2. Therefore, the test scenarios from WP2 will be updated, based on the intermediate results achieved in WP2. This enables a refinement of the test scenarios and a leads to a higher quality of the verification.  The focus of WP 3.2 lies on the analysis of sensor value dependencies and relations. This includes values from a single sensor over time, as well as values from different sensors. The outcome of this analysis is expected to enable a better description and evaluation of the processor behavior and state which can then be exploited for predictive mechanisms in processor architectures. Therefore, a state prediction will be subject of the in depth research. Furthermore, cost functions including parameters with specific weighting factors will be developed. They are used within the models of WP 3.2. The weighting factors are a topic of research and are most probably not constant but dynamic since changing application criticality lead to different behavior of the processor and therefore other dependencies within the processors internal status. The unit of the cost function can be numerical or can be based on time, cycle count, throughput etc. Also these considerations are topic of research in this WP.  **WP 3.2: Algorithmic description of processor data sources relation**  This WP handles the formal and algorithmic, mathematical correct description of the processor data source interrelations and the impact of the processor’s behavior in terms of instruction processing. This WP leads to a set of equations and algorithms and/or pseudo code, which can be used to model highly precise processor models for simulation and especially for runtime prediction of the processor state. As input, the cost functions from WP 3.1 are used and integrated into the algorithms and equations.  **WP 3.3: Information fusion algorithms**  The validation of the feasibility of the information fusion approach will be accomplished. The precision of the simulation results and differences to real-world experiments are determined. If there are significant deviations in the results, the reasons are investigated and measures against them are analyzed and algorithmically included. In the end, the validation process will lead to profound mathematically described knowledge about processor modeling and the prediction of processor behavior and states. Such model descriptions must necessarily be incorporated into the information fusion process for reliable processor state determination. This knowledge is further applicable to increase the precision of processor models and analysis tools in other application fields. | | | |
| **Result** | | | |
| Knowledge formalization of the on-chip evaluation for optimizing the information fusion algorithms and on-chip data acquisition. | | | |

**WP 4: Documentation of scientific results**

|  |  |  |  |
| --- | --- | --- | --- |
| **Staff effort (person months)** | 10 | **Employee** | P1 (100%) and P2 (100%) |
| **Objectives** | | | |
| This WP has the objective to develop the scientific reports and publications based on the project’s research topic. | | | |
| **Description** | | | |
| In parallel to all work packages, documentation will be provided. The publications to the project specific topics are additionally coupled to this WP. During the project, intermediate reports and the final project report will be generated and delivered to the DFG. The reports include a critical assessment of the scientific usability and discussion of possible exploitation scenarios in other and interdisciplinary research fields. | | | |
| **Result** | | | |
| Periodic research report regarding the scientific knowledge gained within the project. Scientific publications in international journals and conferences. | | | |

## Data handling

The research groups involved in this project envision that their investigation is available for further research activities. For this purpose, a repository with all in this project developed models and benchmarks will be made available for the scientific community. This enables the reproduction of the experiments by other researchers and extension to the sequential projects. The project group will provide all data on *Zenodo.org* from where interested researchers are able to download project-related information and code to develop their own experiments.

## Other information

Not available

## Descriptions of proposed investigations involving experiments on humans, human materials or animals

Not applicable in the context of this project proposal.

## Information on scientific and financial involvement of international cooperation partners

Not applicable in the context of this project proposal.

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# Requested modules/funds

## Basic Module

### Funding for Staff

Lehrstuhl für Eingebettete Systeme der Informationstechnik (ESIT):

Request for funding:

1 position as doctoral candidate, E13, for 3 years: 189.980 EUR

2 positions as student researcher, 9h per week, for 3 years: 18.950 EUR

Institut für industrielle Informationstechnik (inIT):

Request for funding:

1 position as doctoral candidate, E13, for 3 years: 189.980 EUR

2 positions as student researcher, 9h per week, for 3 years: 18.950 EUR

### Direct Project Costs

#### Equipment up to 10.000 EUR, Software and Consumables

ESIT: Licenses for HDL simulators and virtual prototyping systems, and consumables: 2.000 EUR per year: 6.000 EUR

inIT: Consumables: 600 EUR per year: 1.800 EUR

#### Travel Expenses

Travel to international conferences:

2 travels per year per group. Travel costs per travel 2.500 EUR: 30.000€

Project meetings. 4 Meetings per year at ESIT or inIT. 2 day meetings. 150 EUR each meeting per involved person. Complete 7.200€

ESIT travel costs: 37.200 EUR

inIT travel costs: 37.200 EUR

These costs include long-term exchange between ESIT and inIT (cf. Section 2.1)

#### Visiting Researchers (excluding Mercator Fellows)

Not applicable

#### Expenses for Laboratory Animals

Not applicable

#### Other Costs

Not applicable

#### Project-related publication expenses

The publication in international journals often requires a publication fee. Especially open source publication comes with not irrelevant costs. To compensate this, the groups request the following funding:

ESIT: 3.000 EUR

inIT: 3.000 EUR

# Project requirements

## Employment status information

The following applicants jointly apply for funding with this project proposal:

Prof. Dr.-Ing. habil. Michael Hübner, Ruhr-Universität Bochum,  
Universitätsstr. 150, 44801 Bochum

Professor (W3), Chairholder “Embedded Systems for Information Technology (ESIT)”

Permanent Contract

Prof. Dr.-Ing. Volker Lohweg, Ostwestfalen-Lippe University of Applied Sciences,  
Institute Industrial IT (inIT), Langenbruch 6, 32657 Lemgo

Professor (C3), Chairholder “Discrete Systems”

Permanent Contract

## First-time proposal data

Not applicable.

## Composition of the project group

On ESIT site, the project is supported by the secretary Ms. Maren Carevic, who will support Prof. Hübner with the administrative organization within the project. Mrs. Carevic has a permanent position at ESIT. Furthermore, the technician Mr. Horst Gass will support the IT administration for all required licensing and tool installation. Mr. Gass has a permanent position as well.

On inIT site, the project is supported by the secretary Ms. Elke Jaschinski, who will support Prof. Lohweg with the administrative organization within the project. Mrs. Jaschinski has a non-permanent position at inIT. Furthermore, the laboratory engineer Mr. Roland Hildebrand will support the technical administration for all required licensing and tool installation. Mr. Hildebrand has a permanent position.

## Cooperation with other researchers

### Researchers with whom you have agreed to cooperate on this project

ESIT:

Prof. Dr.-Ing. Rainer Leupers, RWTH Aachen, Germany

Prof. Dr. Luca Benini, ETH Zürich, Switzerland

inIT:

Prof. Dr. Ralf Salomon, University of Rostock, Germany

Prof. Dr. Oliver Niggemann, Fraunhofer IOSB-INA, Germany

### Researchers with whom you have collaborated scientifically within the past three years

ESIT:

Prof. Dr.-Ing. Jürgen Becker, Karlsruhe Institute of Technology (KIT), Germany

Prof. Dr.-Ing. Andreas Herkersdorf, Technical University Munich (TUM), Germany

inIT:

Prof. Dr. Jürgen Beyerer, Karlsruhe Institute of Technology (KIT), Germany

Prof. Dr. Ralf Salomon, University of Rostock, Germany

Dr. Olaf Enge-Rosenblatt, Fraunhofer IIS, Institutsteil Entwurfsautomatisierung EAS, Germany

## Scientific equipment

ESIT owns a large number of FPGA-based evaluation boards for experiments. The boards are from the main vendors like Altera and Xilinx. A ASIC prototyping system “ChipIT” is available for large scale experiments, e. g., with multicore architectures. ESIT has access to the Tensilica development tools and IP since the chair is certified for Tensilica IP since 2014. Certainly the chair has the standard equipment of PC, servers, and other IT infrastructure.

inIT is equipped with full-range Matlab/Simulink environment. Furthermore, the professorship has a large scale sensor and information fusion system, including necessary sensors and actuators, and signal processing measurement systems from Agilent and other suppliers. Large scale equipment for fusion is available in the SmartFactoryOWL. The research group is equipped with PCs, servers, and IT infrastructure and secure data storage systems.

## Project-relevant cooperation with commercial enterprises

*If applicable, please note the guidelines contained in the EU’s Community Framework for State Aid for Research and Development and Innovation (2006/C 323/01) or contact your research institution in this regard.*

Not applicable in the context of this project proposal.

## Project-relevant participation in commercial enterprises

*Information on connections between the project and the production branch of the enterprise*

Not applicable in the context of this project proposal.

# Additional information

*If applicable, please list proposals requesting major instrumentation and/or those previously submitted to a third party here.*

Not applicable.

1. https://cordis.europa.eu/project/rcn/99931\_en.html, last visit 14.02.2018 [↑](#footnote-ref-2)
2. <http://www.euretile.eu>, last visit 16.06.2017 [↑](#footnote-ref-3)
3. “RISC-V: The Free and Open RISC Instruction Set Architecture,” RISC-V Foundation, https://riscv.org (April 27, 2017) [↑](#footnote-ref-4)
4. „Yocto Project“, Linux Foundation, <https://www.yoctoproject.org/> last visit 16.06.2017 [↑](#footnote-ref-5)
5. „FreeRTOS“, Real Time Engineers Ltd, <http://www.freertos.org/> last visit 16.06.2017 [↑](#footnote-ref-6)